EXHIBIT 4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/391,151	04/22/2019	Hyun Lee	129980-5049-US01	3694

79141 7590 01/10/2020

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
SUN, MICHAEL	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
01/10/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Office Action Summary	Application No. 16/391,151	Applicant(s) Lee et al.	
	Examiner MICHAEL SUN	Art Unit 2183	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 22 April 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 22 April 2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 8/20/2019.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Status of the Application

This Office Action is in response to Applicant's Continuation filed on 4/22/2019.

Claim 1 is pending for this examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 8/20/2019 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Obvious-Type Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van*

Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-12 of

copending Application No. 15/820,076, now U.S. Patent No. 10,268,608, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 15/820,076, now U.S. Patent No. 10,268,608**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal and to

	the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.		perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command

			processing circuit in response to at least one of the module control signals.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608, and as such would be rendered obvious over the already allowed claims of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608.		

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 15/426,064, now U.S. Patent No. 9,824,035**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus;

	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive		a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and memory devices mounted on the module board and configured to perform the first memory' operation in response to the module command signals, the memory devices including a plurality of sets of memory' devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the

	the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.		module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035, and as such would be rendered obvious over the already allowed claims of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035.		

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 14/846,993, now U.S. Patent No. 9,563,587**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of	Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of

	control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of		control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module board including edge connections for connecting to respective ones of the signal lines in the memory bus; memory devices mounted on the module board, including a plurality of sets of memory devices, each respective set of memory devices corresponding to a respective set of the data/strobe signal lines; buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, each respective buffer circuit being coupled between a respective set of the data/strobe signal lines and a corresponding set of memory devices; and a module control device mounted on the module board and configured to receive memory command signals from the memory controller via the set of control/address signal lines and to control the memory devices and the buffer circuits in response to the memory command signals; wherein the each respective buffer circuit is configured to respond to one or more first

	data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.		control signals from the module control device by receiving write data/strobe signals from the respective set of data/strobe signal lines and transmitting the write data/strobe signals to the corresponding set of memory devices during a memory write operation; wherein the each respective buffer circuit is further configured to respond to one or more second control signals from the module control device by receiving read data/strobe signals from the corresponding set of memory devices and transmitting the read data/strobe signals to the memory controller via the respective set of data/strobe signal lines during a memory read operation subsequent to the memory write operation; and wherein the each respective buffer circuit is further configured to time the transmission of the read data/strobe signals during the read operation based on timing information derived from receiving the one or more first control signals and the write data/strobe signals during the write operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587, and as such would be rendered obvious over the already allowed claims of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587.		

Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632. Although the claims at issue are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632, as listed below, and as such anticipate the claims of the copending application:

Claims	**Instant Application**	Claims	**copending Application No. 13/952,599, now U.S. Patent No. 9,128,632**
Independent claim 1	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines, the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus; a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to	Independent claim 1	A memory module to operate in a memory system with a memory controller, the memory system operating according to a system clock, the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to each of the memory command signals; memory devices organized in groups, each group including at

	the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each respective buffer circuit including a delay circuit configured to delay the		least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals; and a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals; and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time, and wherein the each respective buffer circuit is configured to determine a respective time interval based on signals

	respective set of data signals by an amount determined based on at least one of the module control signals.		received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.
Analysis	Examiner points out that the instant claim language is similar to the claim language of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632, and as such would be rendered obvious over the already allowed claims of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632.		

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Manohararajah et al. (US 8,565,033), herein referred to as Manohararajah '033.

Referring to **claim 1,** Manohararajah '033 teaches a memory module operable to communicate with a memory controller via a memory bus (see Fig. 2, wherein memory module 22 communicates with programmable integrated circuit 10 across buses 34 and 36 through memory interface circuitry 24 that includes a memory controller 28), the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data signal lines (see Fig. 2, wherein bus 34 is used for data / data strobe signals and bus 36 is

used for clock / address / commands), the memory module comprising: a module board having edge connections for coupling to respective signal lines in the memory bus (see Fig. 3, wherein the memory modules 22 includes a plurality of memory groups 52 each with respective buss 34 and 36 to connect to programmable integrated circuit 10); a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal (see Fig. 3, wherein memory interface circuitry 24 is used to connect to memory modules 22 and would include circuitry for issuing data / data strobe signals on buses 34 and clock / address / command signals across buses 36); and memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data signal lines (see Figs. 3-5, wherein memory module 22 includes multiple memory groups 52 that connect to memory interface circuit 26 through buses for data / data strobe signals 34 and clock / address / command signals 36, use to perform memory operations utilizing the memory groups 52); and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices, and wherein the each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal, the each

respective buffer circuit including a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals (see Figs. 4-5, I/O circuit 54, read-sync buffers 60, read-valid buffers 62; see Col. 1, lines 57-67, Col. 2, lines 1-5, wherein during read and write operations, buffering can be done to synchronize / tune / calibrate reads and writes, also see Col. 2, lines 37-47; see Col. 2, lines 52-64, wherein delays can be introduced using programmable delay chains to provide additional latency to calibrate operations to a desired tuning accuracy; also see Figs. 14-15, wherein read operations and write operations are calibrated by increasing / reducing latency).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL SUN whose telephone number is (571)270-1724. The examiner can normally be reached on Monday-Friday 8am-4pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aimee Li can be reached on 571-272-4169. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL SUN/
Primary Examiner, Art Unit 2183

Electronically filed April 10, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	3694
Serial No.:	16/391,151	Art Unit:	2183
Filed:	April 22, 2019	Examiner:	Sun, Michael
For:	*MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING*	Attorney Docket No.:	129980-5049-US01

RESPONSE TO OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated January 10, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5049-US01).

Electronic Acknowledgement Receipt

EFS ID:	39130538
Application Number:	16391151
International Application Number:	
Confirmation Number:	3694
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5049-US01
Receipt Date:	10-APR-2020
Filing Date:	22-APR-2019
Time Stamp:	18:25:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5049US01_AMEND.pdf	177364 7ce7cf2b5614a88c12c2a72a8f1333887f7f48	yes	13

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Applicant Arguments/Remarks Made in an Amendment	10	13
Claims	2	9
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:	
Information:	
Total Files Size (in bytes):	177364

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

This amendment responds to the office action mailed January 10, 2020. In the office action, the Examiner:

- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-12 of copending Application No. 15/820,076, now U.S. Patent No. 10,268,608;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-22 of copending Application No. 15/426,064, now U.S. Patent No. 9,824,035;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-20 of copending Application No. 14/846,993, now U.S. Patent No. 9,563,587;
- rejected claim 1 on the ground of nonstatutory double patenting over claims 1-20 of copending Application No. 13/952,599, now U.S. Patent No. 9,128,632; and
- rejected claim 1 as being anticipated by Manohararajah et al. (US 8,565,033).

REMARKS CONCERNING CLAIMS

Claim 1 has been canceled.

Claims 2-21 have been added.

Support for the amendments can be found in at least paragraphs [0034], [0047], [0050], [0052], [0061]-[0074], and [0083]-[0097], and the Figures referenced to in these paragraphs of the application as filed. No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2 - 21.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

I. **REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-12 OF COPENDING APPLICATION NO. 15/820,076, NOW U.S. PATENT NO. 10,268,608**

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

II. **REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-22 OF COPENDING APPLICATION NO. 15/426,064, NOW U.S. PATENT NO. 9,824,035**

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

III. **REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 14/846,993, NOW U.S. PATENT NO. 9,563,587**

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

IV. **REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING OVER CLAIMS 1-20 OF COPENDING APPLICATION NO. 13/952,599, NOW U.S. PATENT NO. 9,128,632**

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 102

V. **REJECTION OF CLAIM 1 AS BEING ANTICIPATED BY MANOHARARAJAH**

Claim 1 has been cancelled. New claims 2-21 are patentable over Manohararajah.

With respect to claim 2, Manohararajah does not disclose or teach all of the elements arranged as claimed. For example, claim 2 recites:

> "a module control device on the module board configurable to ***receive*** input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals."
>
> *Emphasis added.*

Manohararajah does not teach a memory module including such a module control device. In Manohararajah, the memory module 22 is shown to includes memory groups 52-1 to 52-N but no module control device. The memory interface circuitry 24 in Manohararajah, which is on the other side of the buses 34/36, ***outputs*** instead of ***receiving*** input C/A signals corresponding to a memory read operation via the C/A signal lines. Therefore, the memory interface circuitry 24 in Manohararajah cannot be likened to the module control device in claim 2.

As another example, claim 2 further recites:

> "a module board having edge connections to be coupled to respective signal lines in the memory bus" and "data buffers on the module board and coupled ***between*** the edge connections and the memory devices."
>
> *Emphasis added.*

Again, Manohararajah does not teach these claimed features. In Manohararajah, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62, which the Office Action refers to when discussing data buffers, are not coupled between the memory device groups 52-1 to 52-N and any edge connections to be coupled to buses 34/36. Instead, the memory device groups 52-1 to 52-3 are shown in FIGS. 4-5 as coupled directed to one side of the buses 34/36 and the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 are on the other side of the buses 34/36. Thus, Manohararajah does not disclose or teach "data buffers on the module board and coupled ***between*** the edge connections and the memory devices," as recited in claim 2.

As a further example, claim 2 further recites:

> "a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to the module control signals, ... ***transmit*** the first section of the read data to a first section of the data bus."
>
> *Emphasis added.*

In contract, the I/O circuit 54, read-sync buffers 60, and read-valid buffers 62 in Manohararajah ***receive*** read data and read strobes from bus 34 instead of transmitting read data and read strobe to bus 34.

Therefore, Manohararajah does not teach each and every element of claim 2, and claim 2 is patentable over Manohararajah.

Claims 3-14 depend from claim 2 and include further limitations in addition to the limitation in claim 2. Therefore, claims 3-14 are patentable for at least the same reasons claim 2 is patentable.

The arguments regarding claim 2 apply to claim 15. Therefore, claim 15 is also patentable over Manohararajah.

Claims 16-21 depend from claim 15 and include further limitations in addition to the limitation in claim 15. Therefore, claims 16-21 are patentable for at least the same reasons claim 15 is patentable.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 10, 2020

/Jamie J. Zheng/ 51,167

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (New) A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:

a module board having edge connections to be coupled to respective signal lines in the memory bus;

a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;

memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and

data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sample the first section of the read data using the first delayed read strobe; and

transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

3. (New) The memory module of claim 2, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer before the memory read operation.

4. (New) The memory module of claim 3, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer before the memory read operation.

5. (New) The memory module of claim 3, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer before the

memory read operation includes at least another strobe signal associated with the previous operation.

6. (New) The memory module claim 3, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

7. (New) The memory module of claim 2, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation.

8. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

receive the module clock signal;

generate a local clock signal having a programmable phase relationship with the module clock signal; and

output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

9. (New) The memory module of claim 2, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

10. (New) The memory module of claim 9, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

11. (New) The memory module of claim 10, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

12. (New) The memory module of claim 2, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer before the memory read operation.

13. (New) The memory module of claim 2, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

14. (New) The memory module of claim 2, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

15. (New) A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

16. (New) The method of claim 15, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sampling the second section of the read data using the second delayed read strobe; and

transmitting the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based on signals received by the second data buffer before the memory read operation.

17. (New) The method of claim 16, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and

transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer before the memory read operation.

18. (New) The method of claim 16, wherein the signals received by the first data buffer before the memory read operation includes at least a strobe signal associated with a previous operation, and the signals received by the second data buffer before the memory read operation includes at least another strobe signal associated with the previous operation.

19. (New) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

receiving, at the first data buffer, the module clock signal;

generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and

outputting, at the first data buffer, the local clock signal;

receiving, at the first memory device, the local clock signal; and

outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.

20. (New) The method of claim 15, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.

21. (New) The method of claim 20, further comprising, at the first data buffer:

generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;

selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;

selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16391151
Filing Date	22-Apr-2019
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5049-US01
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

( ) Small Entity

( ) Micro Entity

(●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

(●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

( ) A sole inventor

( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

( ) A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16391151
Filing Date:	22-Apr-2019
Title of Invention:	MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5049-US01

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Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
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			Total in USD ($)	160

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☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

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